

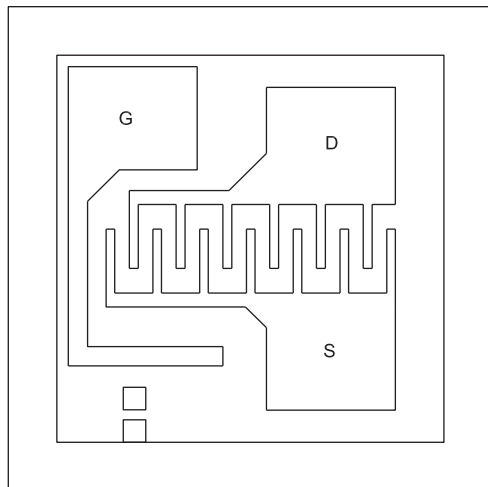
**PROCESS CP210**  
**Small Signal Transistors**  
N - Channel Silicon Amplifier J FET Chip



**PROCESS DETAILS**

Process	EPITAXIAL PLANAR
Die Size	15 x 15 MILS
Die Thickness	8.0 MILS
Drain Bonding Pad Area	3.2 x 4.0 MILS
Source Bonding Pad Area	3.2 x 4.0 MILS
Gate Bonding Pad Area	3.2 x 4.0 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 6,000Å

**GEOMETRY**



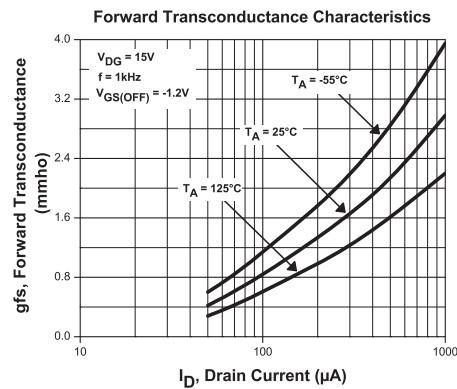
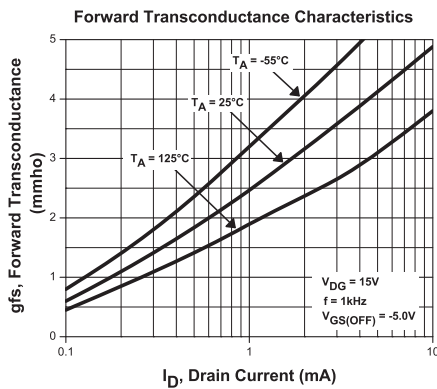
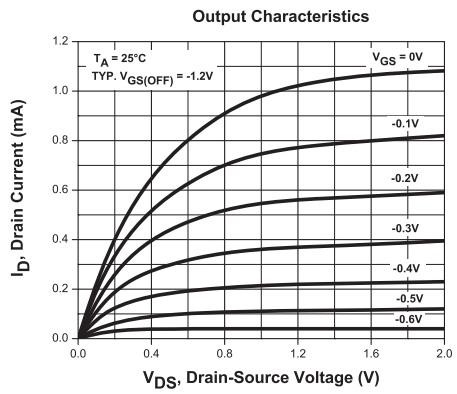
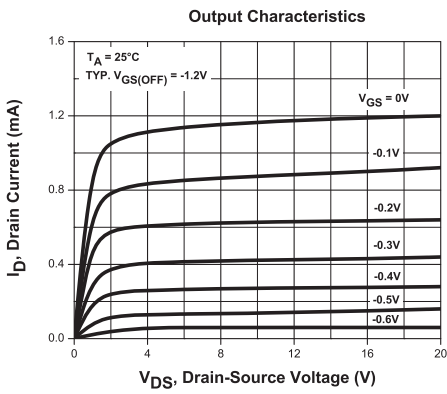
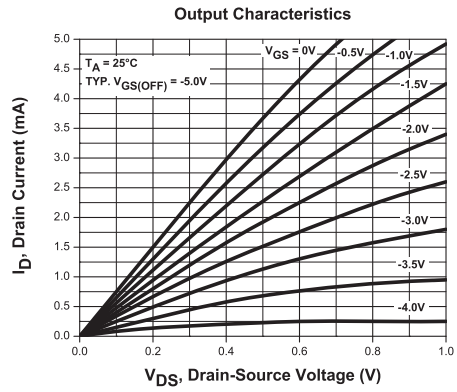
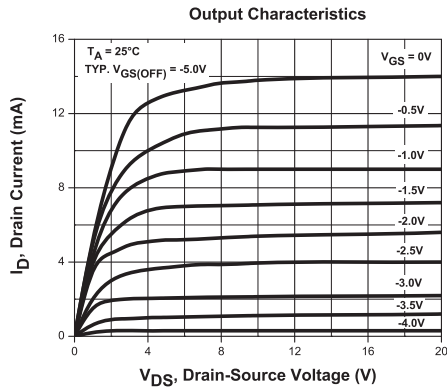
**GROSS DIE PER 4 INCH WAFER**  
53,730

**PRINCIPAL DEVICE TYPES**  
2N4416A  
CMPF4416A

R5 (22-March 2010)

# PROCESS CP210

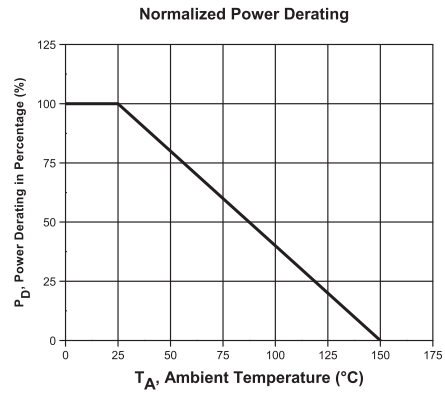
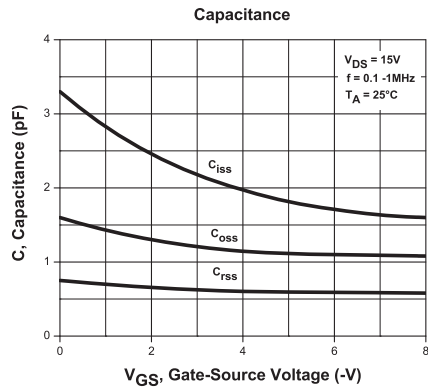
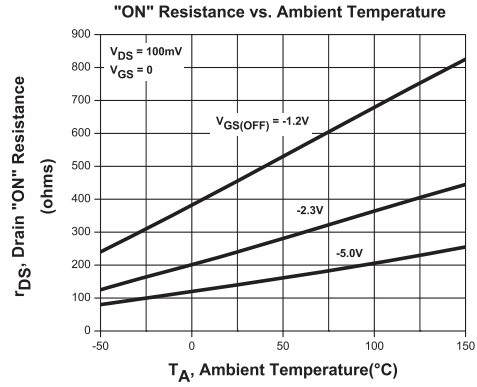
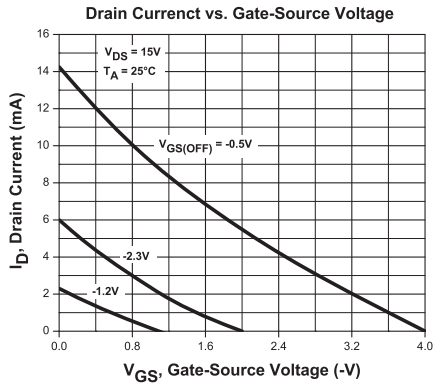
## Typical Electrical Characteristics



R5 (22-March 2010)

# PROCESS CP210

## Typical Electrical Characteristics



R5 (22-March 2010)