ZL30621

3-Output Any Frequency Timing Card PLL with Ultra-Low Jitter

Product Brief

October 2015

Features

- **Low-Bandwidth DPLL**
  - ITU-T G.813/G.8262 compliance (options 1 & 2)
  - Low-jitter operation from any ≥10MHz TCXO
  - Master clock jitter attenuator reduces cost by removing TCXO/OCXO low-jitter requirement
  - Programmable bandwidth, 0.1Hz to 10Hz
  - Attenuates input clock jitter up to several UI
  - Hitless reference switching
  - High-resolution holdover averaging
  - Digitally controlled phase adjustment
- **Input Clocks**
  - Up to 3 inputs, 2 differential/CMOS, one CMOS
  - Any input frequency from 8kHz to 1250MHz (8kHz to 300MHz for CMOS)
  - Per-input activity and frequency monitoring
  - Automatic or manual reference switching
- **Low-Jitter Fractional-N APLL and 3 Outputs**
  - Any output frequency from <1Hz to 1035MHz
  - High-resolution fractional frequency conversion with 0ppm error
  - Encapsulated design requires no external VCXO or loop filter components
  - Each output has independent dividers
  - Output jitter as low as 0.25ps RMS (12kHz-20MHz integration band)

Ordering Information

ZL30621LFG7	64 Pin LGA	Trays
ZL30621LFF7	64 Pin LGA	Tape and Reel

Ni Au

Package size: 5 x 10 mm

-40°C to +85°C

  - Outputs are CML or 2xCMOS, can interface to LVDS, LVPECL, HSTL, SSTL and HCSL
  - In 2xCMOS mode, the P and N pins can be different frequencies (e.g. 125MHz and 25MHz)
  - Per-output supply pin with CMOS output voltages from 1.5V to 3.3V
  - Precise output alignment circuitry and per-output phase adjustment
  - Per-output enable/disable and glitchless start/stop (stop high or low)
- **General Features**
  - Automatic self-configuration at power-up from internal EEPROM; up to four configurations pin-selectable
  - Numerically controlled oscillator mode
  - Input-to-output alignment with external feedback
  - SPI or I^2C processor Interface
  - Easy-to-use evaluation software

Applications

- Telecom timing cards for SONET/SDH, SyncE, wireless base stations and other systems

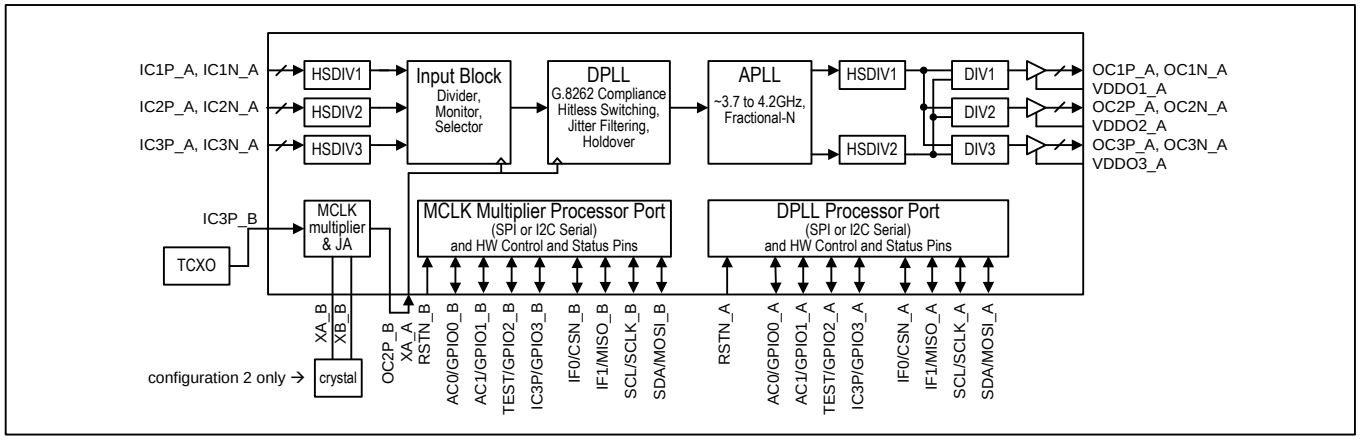


Figure 1 - Functional Block Diagram

1. Application Examples

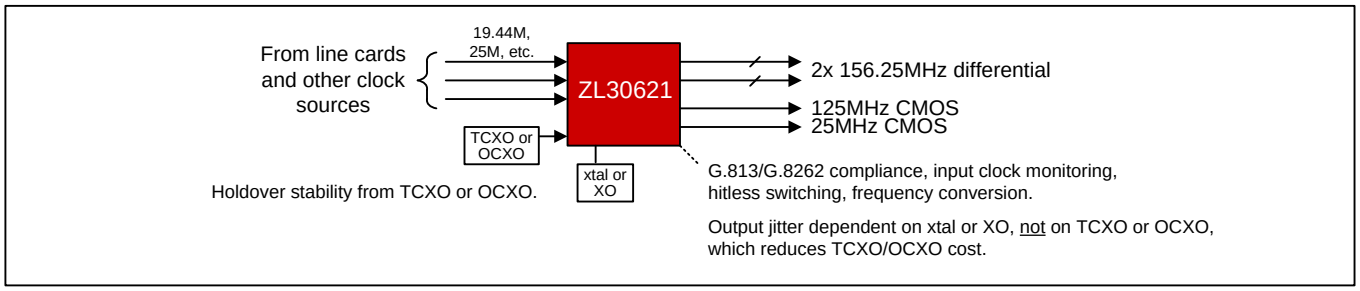


Figure 2 – Telecom Timing Card Application, TCXO + Crystal/XO for Lowest Jitter

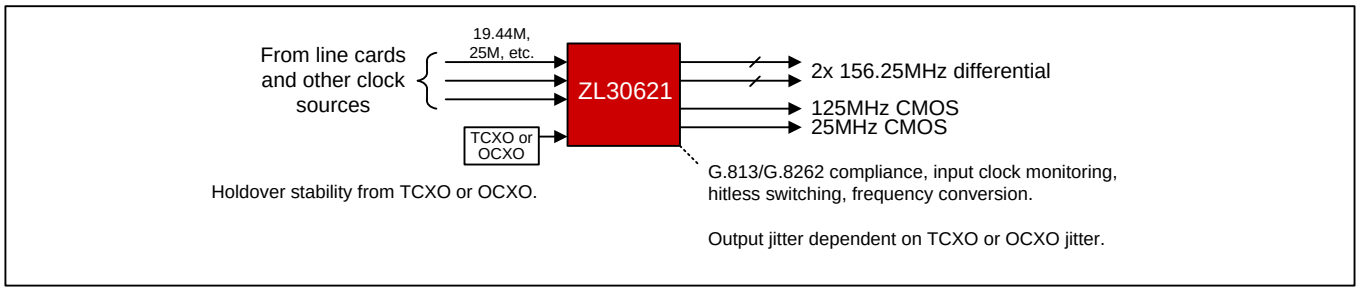


Figure 3 – Telecom Timing Card Application, TCXO Only

2. Detailed Features

2.1 Master Clock Jitter Attenuator and Multiplier

- Enables the DPLL to operate from any TCXO or OCXO ≥ 10MHz regardless of jitter
- When a low-cost crystal or XO is used, output jitter depends on crystal/XO, not on TCXO/OCXO jitter
- Reduces cost by removing tight jitter requirement from TCXO or OCXO

2.2 Input Block Features

- Up to three input clocks, two differential or single-ended, one single-ended
- Input clocks can be any frequency from 8kHz up to 1250MHz (differential) or 300MHz (single-ended)
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN, wireless
- Inputs constantly monitored by programmable activity monitors and frequency monitors
- Fast activity monitor can disqualify the selected reference after a few missing clock cycles
- Frequency measurement and monitoring with 1ppm resolution and accept/reject hysteresis
- Optional input clock invalidation on GPIO assertion to react to LOS signals from PHYs

2.3 DPLL Features

- Very high-resolution DPLL architecture
- State machine automatically transitions between tracking and freerun/holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 0.1Hz to 10Hz
- Less than 0.1dB gain peaking
- Programmable phase-slope limiting
- Programmable tracking range (i.e. hold-in range)
- Truly hitless reference switching with <200ps output clock phase transient
- Output phase adjustment in 10ps steps
- High-resolution frequency and phase measurement
- Fast detection of input clock failure and transition to holdover mode
- Holdover frequency averaging with programmable averaging time and delay time

2.4 APLL Features

- Very high-resolution fractional scaling (i.e. non-integer multiplication)
- Any-to-any frequency conversion with 0ppm error
- Two high-speed dividers (integers 4 to 15, half divides 4.5 to 7.5)
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter components

2.5 Output Clock Features

- Three low-jitter output clocks
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 1Hz to 1035MHz (250MHz max for CMOS and HSTL outputs)
- Output jitter as low as 0.25ps RMS (12kHz to 20MHz)
- In CMOS mode, an additional divider allows the OCxN pin to be an integer divisor of the OCxP pin (Example 1: OC3P 125MHz, OC3N 25MHz. Example 2: OC2P 25MHz, OC2N 1Hz)
- Outputs easily interface with CML, LVDS, LVPECL, HSTL, SSTL, HCSL and CMOS components
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Sophisticated output-to-output phase alignment
- Per-output phase adjustment with high resolution and unlimited range
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)

2.6 General Features

- SPI or I^2C serial microprocessor interface
- Automatic self-configuration at power-up from internal EEPROM memory; pin control to specify one of four stored configurations
- Numerically controlled oscillator (NCO) mode allows system software to steer DPLL frequency with resolution better than 0.01ppb
- Input-to-output alignment with external feedback
- Up to eight general-purpose I/O pins each with many possible status and control options
- Output frame sync signals: 2kHz or 8kHz (SONET/SDH), 1Hz (IEEE 1588) or other frequency
- Internal compensation for local oscillator frequency error

2.7 Evaluation Software

- Simple, intuitive Windows-based graphical user interface
- Supports all device features and register fields
- Makes lab evaluation of the ZL30621 quick and easy
- Generates configuration scripts to be stored in internal EEPROM
- Generates full or partial configuration scripts to be run on a system processor
- Works with or without a ZL30621 evaluation board

3. Pin Diagram

The device is packaged in a 5x10mm 64-pin LGA.

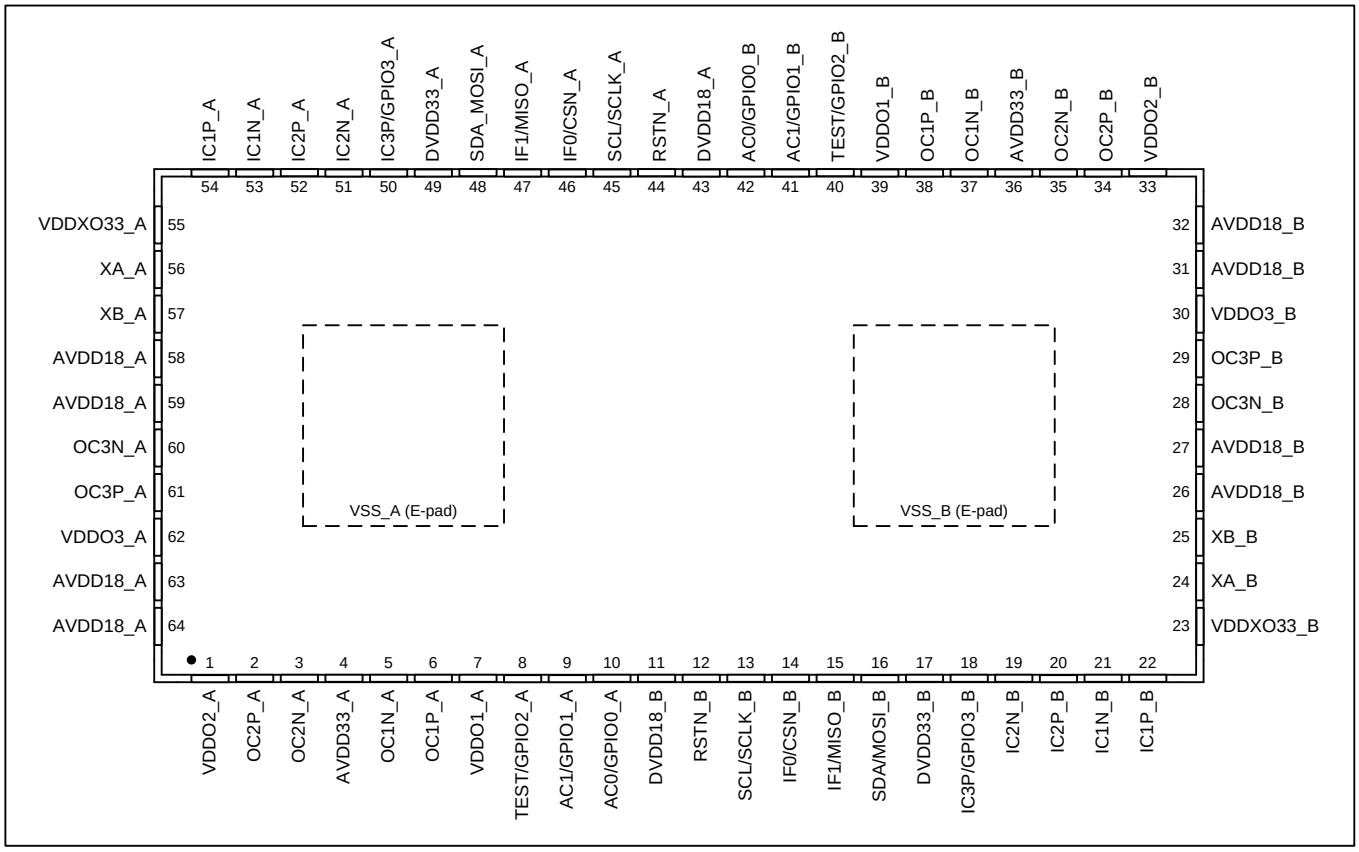
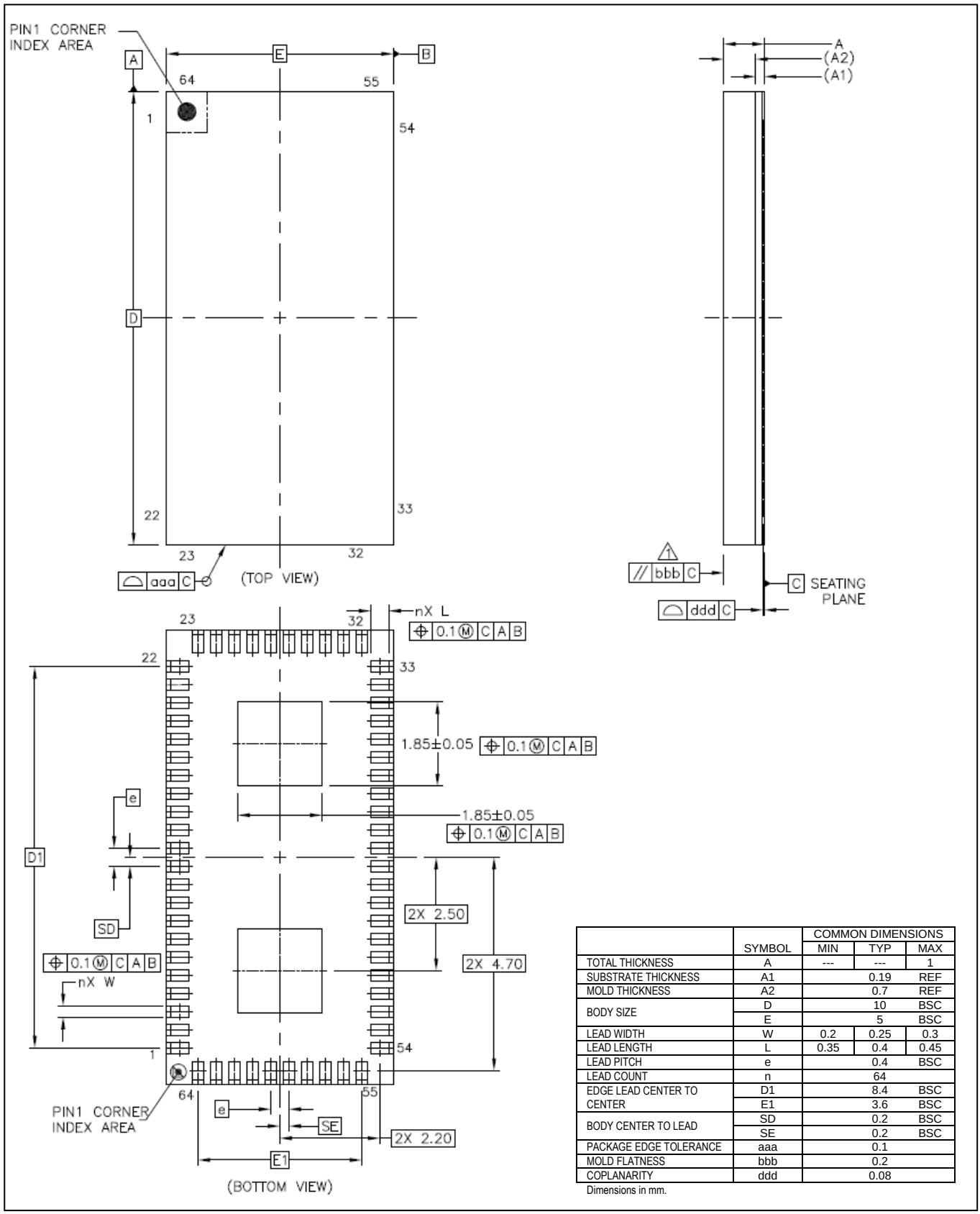


Figure 4 - Pin Diagram

4. Mechanical Drawing



	SYMBOL	COMMON DIMENSIONS		
		MIN	TYP	MAX
TOTAL THICKNESS	A	---	---	1
SUBSTRATE THICKNESS	A1		0.19	REF
MOLD THICKNESS	A2		0.7	REF
BODY SIZE	D		10	BSC
	E		5	BSC
LEAD WIDTH	W	0.2	0.25	0.3
LEAD LENGTH	L	0.35	0.4	0.45
LEAD PITCH	e		0.4	BSC
LEAD COUNT	n		64	
EDGE LEAD CENTER TO CENTER	D1		8.4	BSC
	E1		3.6	BSC
BODY CENTER TO LEAD	SD		0.2	BSC
	SE		0.2	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	

Dimensions in mm.

Microsemi Corporate Headquarters
One Enterprise
Aliso Viejo, CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,400 employees globally. Learn more at **www.microsemi.com**.