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October 2003 Revised January 2005

NC7WP02

TinyLogic® ULP Dual 2-Input NOR Gate

General Description

The NC7WP02 is a dual 2-Input NOR Gate from Fairchild's Ultra Low Power (ULP) series of TinyLogic®. Ideal for applications where battery life is critical, this product is designed for ultra low power consumption within the V_{CC} operating range of 0.9V to 3.6V $V_{CC}.\ \ \,$

The internal circuit is composed of a minimum of inverter stages, including the output buffer, to enable ultra low static and dynamic power.

The NC7WP02 is designed for optimized power and speed, and is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining extremely low CMOS power dissipation.

Features

- Space saving US8 package
- Ultra small MicroPak™ Pb-Free package
- 0.9V to 3.6V V_{CC} supply operation
- 3.6V overvoltage tolerant I/O's at V_{CC} from 0.9V to 3.6V
- t_{PD}

3 ns typ for 3.0V to 3.6V $\rm V_{\rm CC}$

4 ns typ for 2.3V to 2.7V V_{CC}

5 ns typ for 1.65V to 1.95V V_{CC}

6 ns typ for 1.40V to 1.60V V_{CC}

9 ns typ for 1.10V to 1.30V $\ensuremath{V_{CC}}$

24 ns typ for 0.90V $\rm V_{\rm CC}$

- Power-Off high impedance inputs and outputs
- Static Drive (I_{OH}/I_{OL})

±2.6 mA @ 3.00V V_{CC}

 $\pm 2.1~\text{mA}$ @ 2.30V V_{CC}

 ± 1.5 mA @ 1.65V $V_{\mbox{\footnotesize CC}}$

 $\pm 1.0~\text{mA}$ @ 1.40V V_{CC}

 ± 0.5 mA @ 1.10V $V_{\mbox{\footnotesize CC}}$

 $\pm 20~\mu A$ @ 0.9V V_{CC}

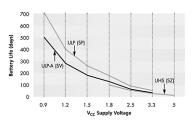
- Low noise switching using design techniques of Quiet Series™ noise/EMI reduction circuitry
- Ultra low dynamic power

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7WP02K8X	MAB08A	WP02	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7WP02L8X	MAC08A	Y4	Pb-Free 8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

Pb-Free package per JEDEC J-STD-020B.

Battery Life vs. V_{CC} Supply Voltage



TinyLogic ULP and ULP-A with up to 50% less power consumption can extend your battery life significantly.

Battery Life = (V_{battery} *I_{battery} *.9)/(P_{device})/24hrs/day

Where, $P_{device} = (I_{CC} * V_{CC}) + (C_{PD} + C_L) * V_{CC}^2 * f$

Assumes ideal 3.6V Lithium Ion battery with current rating of 900mAH and derated 90% and device frequency at 10MHz, with $C_{\rm L}$ = 15 pF load

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Logic Symbol

A₁ ≥1 Y₁
A₂ Y₂
B₂

Pin Descriptions

Pin Names	Description
A _n , B _n	Input
Y _n	Output

Function Table

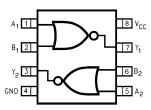
$$Y = \overline{A + B}$$

Inp	Output		
Α	В	Y	
L	L	Н	
L	Н	L	
Н	L	L	
Н	Н	L	

H = HIGH Logic Level L = LOW Logic Level

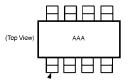
Connection Diagrams

Pin Assignments for US8



(Top View)

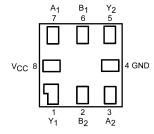
Pin One Orientation Diagram



Pin One

AAA represents Product Code Top Mark - see ordering code **Note**: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak



(Top Through View)

Absolute Maximum Ratings(Note 1)

 $\label{eq:VCC} \begin{array}{ll} \mbox{HIGH or LOW State (Note 2)} & -0.5\mbox{V to V}_{CC} + 0.5\mbox{V} \\ \mbox{V}_{CC} = 0\mbox{V} & -0.5\mbox{V to 4.6\mbox{V}} \\ \mbox{DC Input Diode Current (II_K) V}_{IN} < 0\mbox{V} & \pm 50\mbox{ mA} \\ \end{array}$

DC Output Diode Current (I_{OK})

 $\begin{array}{lll} V_{OUT} > 0V & -50 \text{ mA} \\ V_{OUT} < V_{CC} & +50 \text{ mA} \\ \text{DC Output Source/Sink Current (I}_{OH}/I_{OL}) & \pm 50 \text{ mA} \\ \end{array}$

 $\operatorname{DC}\operatorname{V}_{\operatorname{CC}}$ or Ground Current per

Supply Pin (I_{CC} or Ground) \pm 50 mA Storage Temperature Range (T_{STG}) -65° C to +150 $^{\circ}$ C

Recommended Operating Conditions (Note 3)

Supply Voltage 0.9V to 3.6VInput Voltage (V_{IN}) 0V to 3.6V

Output Voltage (V_{OUT})

HIGH or LOW State $$\rm OV\ to\ V_{CC}$$ $\rm V_{CC}=\rm OV$ $\rm OV\ to\ 3.6V$

Output Current in I_{OH}/I_{OL}

 $V_{CC} = 3.0V \text{ to } 3.6V$ $\pm 2.6 \text{ mA}$ $V_{CC} = 2.3V \text{ to } 2.7V$ $\pm 2.1 \text{ mA}$ $V_{CC} = 1.65V \text{ to } 1.95V$ $\pm 1.5 \text{ mA}$

 $\begin{array}{lll} V_{CC} = 1.40 V \ to \ 1.60 V & \pm 1.0 \ mA \\ \\ V_{CC} = 1.10 V \ to \ 1.30 V & \pm 0.5 \ mA \\ \\ V_{CC} = 0.9 V & \pm 20 \ \mu A \end{array}$

Free Air Operating Temperature (T_A) -40° C to $+85^{\circ}$ C

Minimum Input Edge Rate (Δt/ΔV)

 $V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$ 10 ns/V

Note 1: Absolute Maximum Ratings: are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: IO Absolute Maximum Rating must be observed.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	v _{cc}	$T_A = +25^{\circ}C$		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions
Syllibol	Farameter	(V)	Min	Max	Min	Max	Units	Conditions
V _{IH}	HIGH Level	0.90	0.65 x V _{CC}		0.65 x V _{CC}			
	Input Voltage	$1.10 \le V_{CC} \le 1.30$	0.65 x V _{CC}		0.65 x V _{CC}			
		$1.40 \le V_{CC} \le 1.60$	0.65 x V _{CC}		0.65 x V _{CC}		V	
		$1.65 \leq V_{CC} \leq 1.95$	0.65 x V _{CC}		0.65 x V _{CC}		v	
		$2.30 \leq V_{CC} \leq 2.70$	1.6		1.6			
		$3.00 \le V_{CC} \le 3.60$	2.1		2.1			
V _{IL}	LOW Level	0.90		0.35 x V _{CC}		0.35 x V _{CC}		
	Input Voltage	$1.10 \le V_{CC} \le 1.30$		$0.35 \times V_{\rm CC}$		$0.35 \times V_{\rm CC}$		
		$1.40 \le V_{CC} \le 1.60$		$0.35 \times V_{\rm CC}$		$0.35 \times V_{\rm CC}$	V	
		$1.65 \le V_{CC} \le 1.95$		$0.35 \times V_{\rm CC}$		$0.35 \times V_{\rm CC}$	v	
		$2.30 \leq V_{CC} \leq 2.70$		0.7		0.7		
		$3.00 \leq V_{CC} \leq 3.60$		0.9		0.9		
V _{OH}	HIGH Level	0.90	V _{CC} - 0.1		V _{CC} - 0.1			
	Output Voltage	$1.10 \le V_{CC} \le 1.30$	V _{CC} - 0.1		V _{CC} - 0.1			
		$1.40 \le V_{CC} \le 1.60$	V _{CC} - 0.1		V _{CC} - 0.1			I _{OH} = -20 μA
		$1.65 \le V_{CC} \le 1.95$	V _{CC} - 0.1		V _{CC} - 0.1			ΙΟΗ – –20 μΑ
		$2.30 \leq V_{CC} \leq 2.70$	V _{CC} - 0.1		V _{CC} - 0.1			
		$3.00 \leq V_{CC} \leq 3.60$	V _{CC} - 0.1		V _{CC} - 0.1		V	
		$1.10 \le V_{CC} \le 1.30$	0.75 x V _{CC}		0.70 x V _{CC}			$I_{OH} = -0.5 \text{ mA}$
		$1.40 \le V_{CC} \le 1.60$	1.07		0.99			$I_{OH} = -1.0 \text{ mA}$
		$1.65 \le V_{CC} \le 1.95$	1.24		1.22			$I_{OH} = -1.5 \text{ mA}$
		$2.30 \le V_{CC} \le 2.70$	1.95		1.87			I _{OH} = -2.1 mA
		$3.00 \le V_{CC} \le 3.60$	2.61		2.55			I _{OH} = -2.6 mA

DC Electrical Characteristics (Continued)

Symbol	Parameter	V _{CC}	T _A =	+25°C	T _A = -40°C to +85°C		Units	Conditions
Cynibol	i di dilletei	(V)	Min Max		Min Max		Onics	Conditions
V _{OL}	LOW Level	0.90		0.1		0.1		
	Output Voltage	$1.10 \le V_{CC} \le 1.30$		0.1		0.1		
		$1.40 \leq V_{CC} \leq 1.60$		0.1		0.1		I - 20 ·· A
		$1.65 \leq V_{CC} \leq 1.95$		0.1		0.1		$I_{OL} = 20 \mu A$
		$2.30 \leq V_{CC} \leq 2.70$		0.1		0.1		
		$3.00 \leq V_{CC} \leq 3.60$		0.1		0.1	V	
		$1.10 \le V_{CC} \le 1.30$		0.30 x V _{CC}		0.30 x V _{CC}		I _{OL} = 0.5 mA
		$1.40 \le V_{CC} \le 1.60$		0.31		0.37		I _{OL} = 1.0 mA
		$1.65 \le V_{CC} \le 1.95$		0.31		0.35		I _{OL} = 1.5 mA
		$2.30 \le V_{CC} \le 2.70$		0.31		0.33		I _{OL} = 2.1 mA
		$3.00 \leq V_{CC} \leq 3.60$		0.31		0.33		I _{OL} = 2.6 mA
I _{IN}	Input Leakage Current	0.90 to 3.60		±0.1		±0.5	μΑ	$0 \le V_I \le 3.6V$
I _{OFF}	Power Off Leakage Current	0		0.5		0.5	μΑ	$0 \le (V_1, V_0) \le 3.6V$
I _{CC}	Quiescent Supply Current	0.90 to 3.60		0.9		0.9	μΑ	$V_I = V_{CC}$ or GND

AC Electrical Characteristics

Symbol	Parameter	V _{CC}	T _A = +25°C		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions	Figure	
Syllibol	Parameter	(V)	Min	Тур	Max	Min	Max	Units	Conditions	Number
t _{PHL}	Propagation Delay	0.90		24.0						
t _{PLH}		$1.10 \le V_{CC} \le 1.30$	4.0	9.0	20.7	3.5	30.9			
		$1.40 \le V_{CC} \le 1.60$	2.0	6.0	12.4	1.5	13.9	ns	C _L = 10 pF	Figures
		$1.65 \leq V_{CC} \leq 1.95$	1.5	5.0	9.6	1.0	12.1	115	$R_L = 1 M\Omega$	1, 2
		$2.30 \leq V_{CC} \leq 2.70$	1.0	4.0	7.0	8.0	8.0			
		$3.00 \leq V_{CC} \leq 3.60$	1.0	3.0	5.7	0.5	6.9			
t _{PHL}	Propagation Delay	0.90		27.0						
t _{PLH}		$1.10 \le V_{CC} \le 1.30$	5.0	10.0	22.2	4.5	33.9			Figures 1, 2
		$1.40 \leq V_{CC} \leq 1.60$	3.0	7.0	13.3	2.5	16.0	ns	C _L = 15 pF	
		$1.65 \le V_{CC} \le 1.95$	2.0	5.0	10.3	2.0	12.6	115	$R_L = 1 M\Omega$	
		$2.30 \leq V_{CC} \leq 2.70$	1.5	4.0	7.4	1.0	8.2			
		$3.00 \leq V_{CC} \leq 3.60$	1.0	3.0	6.1	0.5	7.0			
t _{PHL}	Propagation Delay	0.90		34.0						
t _{PLH}		$1.10 \le V_{CC} \le 1.30$	6.0	12.0	26.0	5.0	43.0			
		$1.40 \le V_{CC} \le 1.60$	4.0	8.0	16.0	3.0	18.0	ns	C _L = 30 pF	Figures
		$1.65 \le V_{CC} \le 1.95$	2.0	6.0	12.0	2.0	14.0	113	$R_L = 1 M\Omega$	1, 2
		$2.30 \leq V_{CC} \leq 2.70$	1.0	5.0	9.0	1.0	10.0			
		$3.00 \leq V_{CC} \leq 3.60$	0.8	4.0	7.0	0.5	8.9			
C _{IN}	Input Capacitance	0		2.0				pF		
C _{OUT}	Output Capacitance	0	•	4.0			•	pF		
C _{PD}	Power Dissipation Capacitance	0.9 to 3.60		6.0				pF	$V_I = 0V \text{ or } V_{CC},$ f = 10 MHz	

AC Loading and Waveforms

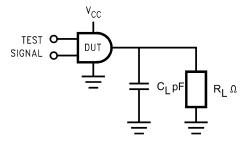


FIGURE 1. AC Test Circuit

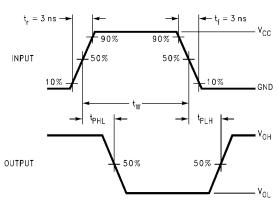


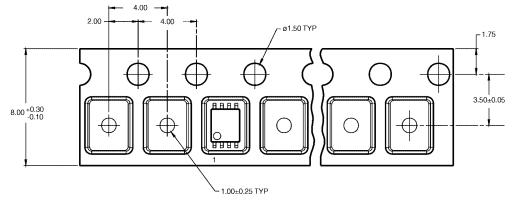
FIGURE 2. AC Waveforms

Symbol	V _{cc}								
- Cyz-:	$3.3V \pm 0.3V$	$\textbf{2.5V} \pm \textbf{0.2V}$	1.8V \pm 0.15V	1.5V ± 0.10V	1.2V ± 0.10V	0.9V			
V _{mi}	1.5V	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2			
V _{mo}	1.5V	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2			

Tape and Reel Specification TAPE FORMAT for US8

1741 = 1 014111741 101 4	, , , , , , , , , , , , , , , , , , , 			
Package	Tape	Number	Cavity	Cover Tape
Designator	Section	Cavities	Status	Status
	Leader (Start End)	125 (typ)	Empty	Sealed
K8X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

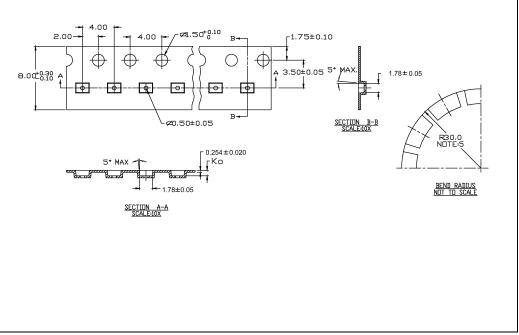
TAPE DIMENSIONS inches (millimeters)

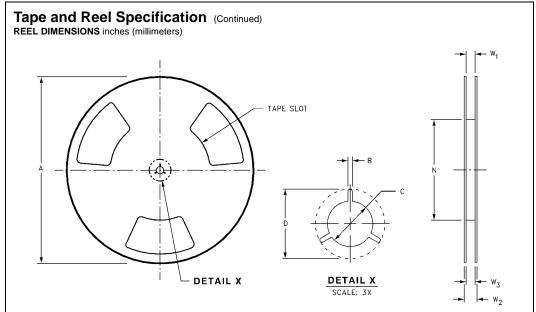


TAPE FORMAT for MicroPak

Package	Tape	Number	Cavity	Cover Tape	
Designator	Section	Cavities	Status	Status	
	Leader (Start End)	125 (typ)	Empty	Sealed	
L8X	Carrier	3000	Filled	Sealed	
	Trailer (Hub End)	75 (typ)	Empty	Sealed	

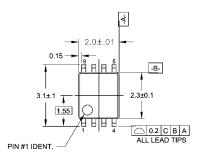
TAPE DIMENSIONS inches (millimeters)

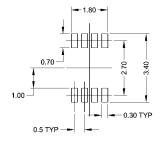




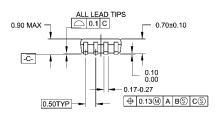
	Tape Size	Α	В	С	D	N	W1	W2	W3
	0 mm	7.0	0.059	0.512	0.795	2.165	0.331 + 0.059/-0.000	0.567	W1 + 0.078/-0.039
8 mm	OIIIII	(177.8)	(1.50)	(13.00)	(20.20)	(55.00)	(8.40 + 1.50/-0.00)	(14.40)	(W1 + 2.00/-1.00)

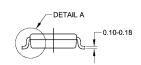
Physical Dimensions inches (millimeters) unless otherwise noted

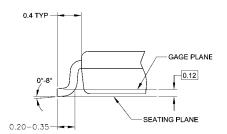




LAND PATTERN RECOMMENDATION







NOTES:

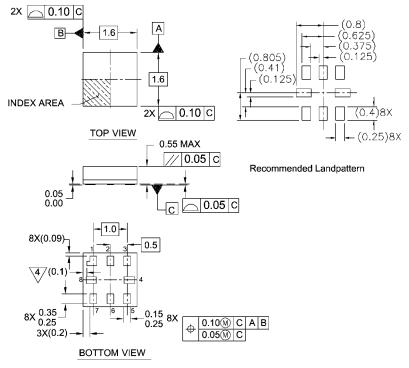
- A. CONFORMS TO JEDEC REGISTRATION MO-187
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

DETAIL A

MAB08AREVC

8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide Package Number MAB08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

- 1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
- 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y.14M-1994
- 4/PIN 1 FLAG, END OF PACKAGE OFFSET.

MAC08AREVC

Pb-Free 8-Lead MicroPak, 1.6 mm Wide Package Number MAC08A

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